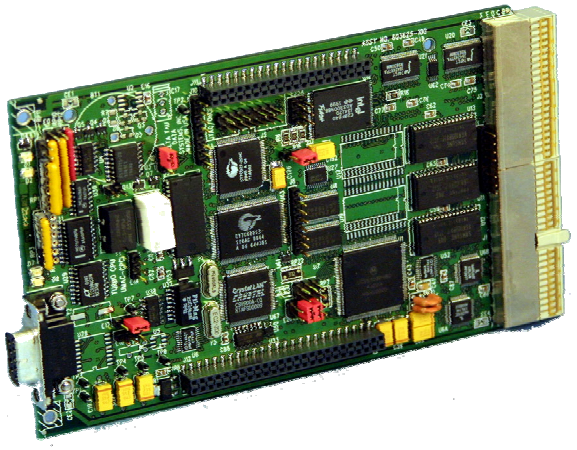
HARDWARE REFERENCE MANUAL

UMAC-CPCI
Turbo CPU Board



Turbo CPU Board

4Ax-603625-xUxx

January 28, 2003

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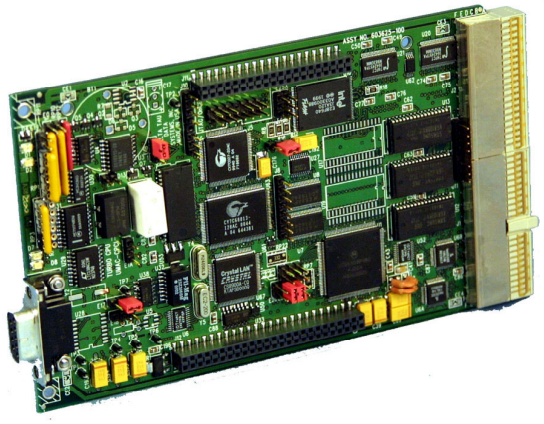
INTRODUCTION

Delta Tau's UMAC-CPCI systems provide a compact and clean integration of motion and I/O control for sophisticated automation equipment. The system consists of a modular set of 3U-size (100mm x 160mm) boards in the "Compact PCI" format, implementing Turbo PMAC software and hardware functions, communicating with each other over a common backplane (the "Compact UBUS"). All field wiring is available on rear connectors, suitable for a user-designed distribution system to the machine. UMAC (Universal Motion and Automation Controller) -CPCI systems provide integrated connectivity as well as ease of assembly, diagnostics, and repair. UMAC-CPCI systems differ from "standard" UMAC systems in that all field wiring comes to the back of the rack, behind the backplane, instead of direct top and bottom access.

The UMAC-CPCI Turbo CPU board (Part number 3A0-603625-10x) implements a Turbo PMAC2 CPU in the 3U CPCI form factor. Its software operation is completely identical to other Turbo PMAC2 controllers.

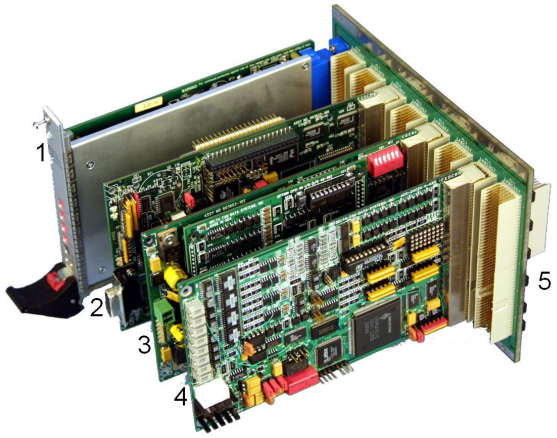
Note that a Compact PCI interface does not automatically come with a UMAC-CPCI system, nor is one necessary to communicate to the system, given the other possible communications ports: RS-232, RS-422, USB, and Ethernet.

This picture shows the UMAC-CPCI Turbo CPU board. The connectors on the right side plug into the "Compact UBUS" backplane board, with the bottom right connector being the bus connector, and the top right connector containing the external "field wiring" signals, which typically pass through the backplane board. The connector at lower left is an RS-232 port intended for setup and diagnostics; the stack connectors top and bottom provide the link to a CPCI "bridge board".



This picture shows a sample configuration of a UMAC-CPCI system, not installed in its rack. It consists of the following components:

1. Rack power supply (not a Delta Tau product)
2. UMAC-CPCI CPU board
3. ACC-11C Sinking I/O board
4. ACC-24C2A analog axis interface board
5. ACC-C8 8-slot Compact UBUS backplane. Note the "pass-through" connector on the back for field-wiring distribution. In this picture, alternate slots in the backplane have been left open to make each board more visible. This does not have to be done in actual use.



Associated Manuals

This document is the Hardware Reference Manual for the UMAC-CPCI Turbo CPU board for an UMAC-CPCI system. It describes the hardware features and provides setup instructions.

You will need other manuals as well to use your UMAC-CPCI system. Each accessory to the UMAC-CPCI Turbo CPU board has its own manual, describing its operation and any required software setup of the Turbo CPU.

You will also need the Software Reference Manual for the Turbo PMAC family, and the User Guide for the PMAC or Turbo PMAC families.

BOARD CONFIGURATION

The base version of the UMAC-CPCI Turbo CPU board provides a 1-slot 3U-format Eurocard board with:

- 80 MHz DSP56303 CPU (120 MHz PMAC equivalent)
- 128k x 24 SRAM compiled/assembled program memory (Opt. 5C0)
- 128k x 24 SRAM user data memory (Opt. 5C0)
- 1M x 8 flash memory for user backup & firmware (Opt. 5C0)
- Latest released firmware version
- RS-232/422 serial interface, available both on front-panel DB-9 connector and on backside field-wiring connector
- Backplane Compact UBUS expansion connector for communication to servo and I/O accessory boards
- Backside field-wiring connector

Option 1: Communications Interfaces

The UMAC-CPCI Turbo CPU board comes standard only with an RS-232/422 serial interface. The Option 1 family provides faster interfaces for high-speed communications – Universal Serial Bus (USB), Ethernet, or the link to the CPCI bus through a "bridge" daughter board.

- Option 1: On-board 10-Base-T TCP/IP Ethernet interface. The key added components are U67 and U32.
- Option 1A: On-board 12 Mbit/sec USB interface. The key added component is U67.
- Option 1B: Solder-side stack connectors to CPCI-bridge daughter board. This option should only be ordered when the bridge board is to be installed on the left side of the CPU board, so the CPU board is in the leftmost slot of the Compact UBUS backplane, and the bridge board is in the rightmost slot of the Compact PCI bus backplane.

Option 2: Dual-Ported RAM

With either the Option 1 Ethernet interface, or the Option 1A USB interface, communications throughput can be increased through the use of dual-ported RAM, which provides a bank of memory that can be directly accessed by both the UMAC-CPCI Turbo CPU and the communications microcontroller.

- Option 2: 32k x 16 bank of on-board dual-ported RAM (requires Option 1 or 1A) in component U56.

Option 5: CPU and Memory Configurations

The various versions of Option 5 provide different CPU speeds and main memory sizes on the piggyback CPU board. Only one Option 5xx may be selected for the board.

The CPU is a DSP563xx IC as component U1. It is currently available only as an 80 MHz or 100 MHz device (with computational power equivalent to a 120 MHz or 150 MHz non-Turbo PMAC, respectively), but higher speed versions may become available.

The compiled/assembled-program ("P") memory SRAM ICs are located in U14, U15, and U16. These ICs form the active memory for the firmware, compiled PLCs, and user-written phase/servo algorithms. These can be 128k x 8 ICs (for a 128k x 24 bank), fitting in the smaller footprint, or they can be the larger 512k x 8 ICs (for a 512k x 24 bank), fitting in the full footprint.

The user-data memory ("X/Y") SRAM ICs are located in U11, U12, and U13. These ICs form the active memory for user motion programs, uncompiled PLC programs, and user tables and buffers. These can be 128k x 8 ICs (for a 128k x 24 bank), fitting in the smaller footprint, or they can be the larger 512k x 8 ICs (for a 512k x 24 bank), fitting in the full footprint.

The flash memory IC is located in U10. This IC forms the non-volatile memory for the board's firmware, the user setup variables, and for user programs, tables, and buffers. It can be 1M x 8, 2M x 8, or 4M x 8 in capacity.

- Option 5C0 is the standard CPU and memory configuration. It is provided automatically if no Option 5xx is specified. It provides an 80 MHz DSP56303 CPU (120 MHz PMAC equivalent) with 8k x 24 of internal memory, an external 128k x 24 of compiled/assembled program memory, an external 128k x 24 of user data memory; and a 1M x 8 flash memory. Setup variable I52 should be set and saved at 7 for 80 MHz operation.
- Option 5C3 provides an 80 MHz DSP56303 CPU (120 MHz PMAC equivalent) with 8k x 24 of internal memory, an expanded external 512k x 24 of compiled/assembled program memory, an expanded external 512k x 24 of user data memory, and a 4M x 8 flash memory. Setup variable I52 should be set and saved at 7 for 80 MHz operation.
- Option 5D0 provides a 100 MHz DSP56309 CPU (150 MHz PMAC equivalent) with 34k x 24 of internal memory, an external 128k x24 of compiled/assembled program memory, an external 128k x 24 of user data memory; and a 1M x 8 flash memory. Setup variable I52 should be set and saved at 9 for 100 MHz operation.
- Option 5D3 provides a 100 MHz DSP56309 CPU (150 MHz PMAC equivalent) with 34k x 24 of internal memory, an expanded external 512k x 24 of compiled/assembled program memory, an expanded external 512k x 24 of user data memory, and a 4M x 8 flash memory. Setup variable I52 should be set and saved at 9 for 100 MHz operation.

Option 8: High-Accuracy Clock Crystal

The UMAC-CPCI Turbo CPU board has a clock crystal (component Y1) of nominal frequency 19.6608 MHz (~20 MHz). The standard crystal's accuracy specification is +/-100 ppm.

- Option 8A provides a nominal 19.6608 MHz crystal with a +/-15 ppm accuracy specification.

Option 9: Serial Port Configuration

The UMAC-CPCI Turbo CPU board comes standard with a single RS-232/422 serial port, a second serial port can be added.

- Option 9T adds an auxiliary RS-232 port on the CPU board. The key components added are ICs U28 and U43.

Option 10: Firmware Revision Specification

Normally the UMAC-CPCI Turbo CPU board is provided with the newest released firmware revision. Some users may wish to "freeze" their designs on an older revision. A label on the U10 flash memory IC shows the firmware revision loaded at the factory. The **VERSION** command can be used to report what firmware revision is currently installed.

- Option 10 provides for a user-specified firmware version.

Option 16: Battery-Backed Parameter Memory

The contents of the standard memory are not retained through a power-down or reset unless they have been saved to flash memory first. Option 16 provides supplemental battery-backed RAM for real-time parameter storage that is ideal for holding machine state parameters in case of an unexpected power-down.

- Option 16A provides a 32k x 24 bank of battery-backed parameter RAM in components U17, U18, and U19 and a "can-stack" lithium battery in component BT1. While the average expected battery life is over five years, a yearly replacement schedule is recommended. Replacement batteries can be ordered from Delta Tau as Acc-1LS (Part # 100-0QTC85-000).

HARDWARE SETUP

Clock-Source Jumpers

In order to operate properly, the Turbo CPU board must receive servo and phase clock signals from a source external to the board. These clock signals can be brought into the board from one of three possible ports: the stack connector, the UBUS backplane connector, or the front-side main serial-port connector. Jumpers E1A and E1B must be configured properly for the clock source used.

(Note: If the UMAC-CPCI Turbo CPU board cannot find the clock signal from the source specified by these jumpers, it will generate its own 2.26kHz servo clock and its own 9.04kHz phase clock so it will stay in operation.)

To receive the clock signals over the Compact-UBUS backplane, usually from an ACC-24C2x axis-interface board, E1A must connect pins 1 and 2, and E1B must connect pins 2 and 3. This configuration is typical for an UMAC-CPCI system. The clock signals are output on the main serial port.

To receive the clock signals through the stack connectors, usually from the MACRO IC on the CPCI "bridge" board, E1A must connect pins 1 and 2, and the E1B jumper must be removed. The clock signals are output on the main serial port.

To receive the clock signals through the main serial port, usually from another UMAC system or a reference signal generator, E1A must connect pins 2 and 3, and E1B must connect pins 1 and 2. This configuration is rarely used, but permits complete synchronization to the system that is generating the clock signals.

Watchdog Timer Jumper

Jumper E19 should be OFF for normal operation, leaving the watchdog timer circuit active and prepared to shut down the card in case of a severe problem. Putting jumper E19 ON disables the watchdog timer circuit. This should only be used for test purposes, in trying to track down the source of watchdog timer trips. Normal operation of a system with this jumper ON should never be attempted, as an important safety feature is disabled.

Operation Mode Jumpers

Jumpers E20, E21, and E22 control the operational mode of the UMAC-CPCI Turbo CPU. For normal operation, E20 must be OFF, E21 must be ON, and E22 must be ON. Other settings of these jumpers are for factory use only.

Firmware Reload Jumper

Jumper E23 should be OFF for normal operation. If you want to load new firmware into the flash-memory IC on the CPU, E23 should be ON when the card is powered up. This puts the card in "bootstrap mode", ready to accept new firmware. If you then try to establish communications to the card with the Executive program, either over the main serial port or the optional USB or Ethernet ports, the Executive program will automatically recognize that the card is in bootstrap mode, and prompt you for the firmware file to download.

Re-Initialization Jumper

Jumper E3 should be OFF for normal operation, where the last saved I-variable values are loaded from flash memory into active memory at power-up/reset. If E3 is ON during power-up/reset, the factory default I-variable values are instead loaded into active memory at power-up/reset. The last saved values are not lost when this happens. This jumper is typically only used when the system's set up has a problem severe enough that communications does not work – otherwise, a **$$$***** command can be used for re-initialization.

Serial-Port Level Select Jumpers

The standard serial port can be used for either RS-232 or RS-422 serial communications. To use RS-232, jumpers E17 and E18 should connect pins 1 and 2; to use RS-422, jumpers E17 and E18 should connect pins 2 and 3. The front-panel DB-9 serial connector provides only the RS-232 signals, so in order to use this connector, E17 and E18 must both connect pins 1 and 2.

DPRAM IC Select Jumper

The UMAC-CPCI Turbo CPU board can provide dual-ported RAM (DPRAM) communications using either the on-board Option 2B DPRAM IC through the USB or Ethernet port, or using the DPRAM IC on the CPCI bridge daughter board through that board's CPCI port. Jumper E24 must connect pins 1 and 2 to use the on-board Option 2B DPRAM; it must connect pins 2 and 3 to use the CPCI bridge board DPRAM.

Flash IC Firmware Bank Select Jumpers

Some makes of the U10 flash memory IC on the UMAC-CPCI Turbo CPU board can store multiple versions of the operating firmware inside. Jumpers E25A, E25B, and E25C select which bank is loaded into active memory on a normal power-up/reset, and which bank will be written to if the board is powered up or reset with the E23 jumper on.

The eight possible settings of these three jumpers provide eight banks for the firmware. A standard production version of the UMAC-CPCI Turbo CPU board is shipped with firmware loaded only in the bank selected by having all three of these jumpers OFF.

Flash IC Power Supply Select Jumper

Jumper W1 is set at the factory for the voltage level of the flash IC installed in U10. It connects pins 1 and 2 for a 3.3V flash IC; it connects pins 2 and 3 for a 5V flash IC. Even if this is a removable, not soldered, jumper, it should not be changed by the user.

Power-Supply Check Select Jumper

The UMAC-CPCI Turbo CPU board has a circuit to evaluate the voltage levels received through the J1 Compact UBUS backplane connector. This circuit can then notify other boards in the system (without software intervention) of a bad supply, so the outputs of those boards are automatically shut down. Jumper E11 should be OFF if only the 5V supply is checked for this purpose; it should be ON if the +12V and –12V backplane supplies are to be checked for this purpose. Note that many users will provide a separate isolated +/-12V supply into the analog axis boards, and each analog axis board has its own power-supply check circuit.

Reset-Lock Jumper

Putting jumper E0 ON locks the UMAC-CPCI Turbo CPU board in the reset state. This setting permits the loading of logic into the programmable ICs on the board and is for factory use only. This jumper should be OFF for all normal operation.

CONNECTIONS

In a typical installation, the UMAC-CPCI Turbo CPU board is simply slid into a slot of a 3U-Eurocard rack until it inserts into the mating connectors on the backplane board already installed in the rack. In actual operation, all signals to the board come into the CPU board through the backplane. (The front-panel RS-232 connector is intended for test and debugging purposes.)

Compact UBUS Connector

The J1 "Compact UBUS" connector at the bottom of the back edge of the board provides the means for the UMAC-CPCI Turbo CPU board to communicate with axis and I/O boards through a common backplane board, such as a Delta Tau ACC-Cx board, or a user-designed backplane board. It also provides the 3.3V and 5V power supply lines to the CPU board.

Because of the design of the Compact UBUS, the CPU board can operate in any slot of the bus. However, if the CPU board has the CPCI bridge board installed on it, the CPU board must be installed in the end slot of the Compact UBUS backplane immediately adjacent to the Compact PCI bus backplane board, so the bridge board can be installed in the adjacent CPCI end slot.

Rear Field Wiring Connector

The J2 field-wiring connector at the top of the back edge of the board provides the path for all of the signals between the CPU board and the outside system. In a typical configuration, this connector is mated with a "pass-through" connector on the Compact UBUS backplane board, and a system-specific distribution system is installed behind the backplane.

The J2 connector contains the signals for the main serial port (either RS-232 or RS-422 levels), the optional auxiliary RS-232 serial port, the optional USB port, and the optional Ethernet port. It also provides the outputs of the relay for the CPU board's watchdog timer.

Front-Panel RS-232 Connector

The J4 DB-9S connector on the front panel is a standard RS-232 connector for the main serial port into the CPU, permitting a straight-across cable to a matching cable on a host computer. Jumpers E17 and E18 must each connect pins 1 and 2 to permit use of this connector. These same signals are available on the rear J2 connector; this front connector is intended for setup and diagnostic use more than use in the actual application.

Stack Connectors to Bridge Board

Stacking socket connectors J11 and J12 on the top and bottom edges, respectively, of the component side of the CPU board provide connection to the optional CPCI bridge board that can form a two-board "stack" with the CPU board. (Mating prong connectors on the solder side of the bridge board must be ordered.) In this configuration, the UMAC-CPCI Turbo CPU board can be installed in the rightmost slot of a Compact UBUS backplane, and the bridge board can be installed in the leftmost slot of a CPCI backplane.

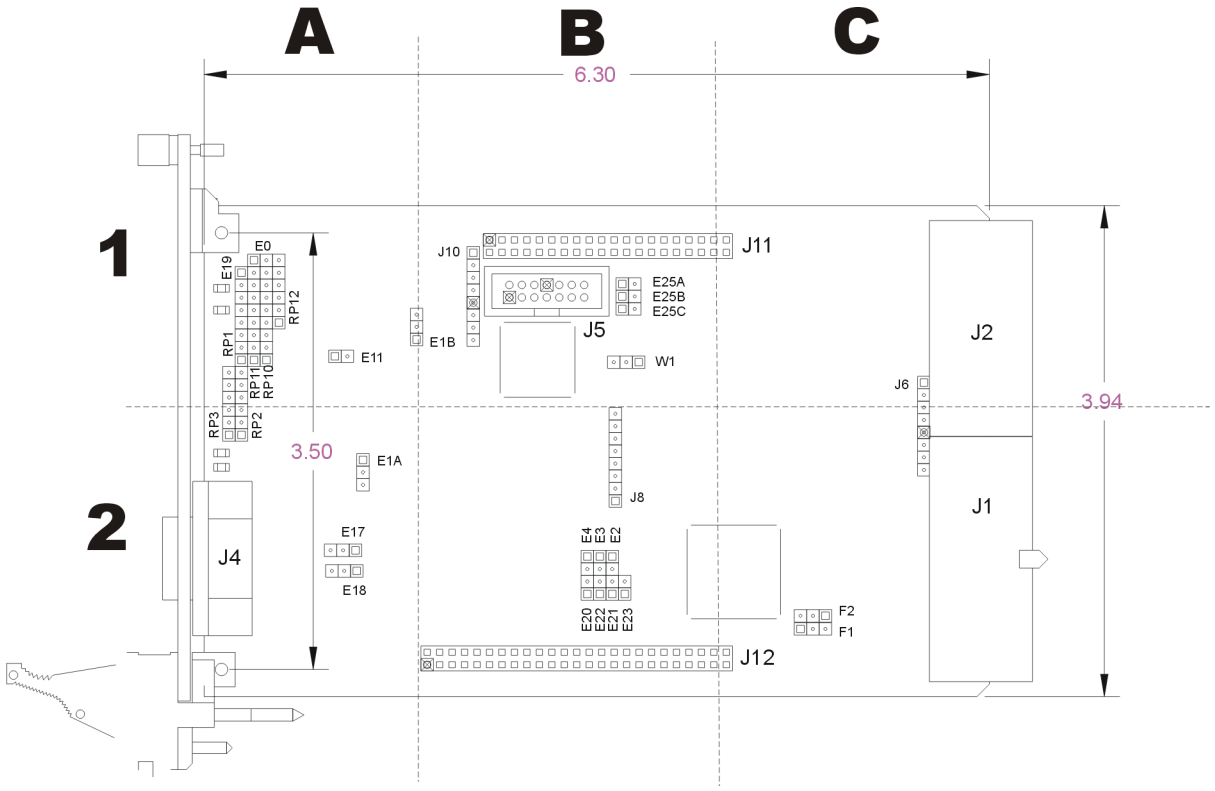
If Option 2C is ordered, stacking "prong" connectors J11A and J12A are provided at the same locations on the solder side of the board. These provide connection to mating socket connectors on the component side of the bridge board. In this configuration, the UMAC-CPCI Turbo CPU board can be installed in the leftmost slot of a Compact UBUS backplane, and the bridge board can be installed in the rightmost slot of a CPCI backplane.

Factory-Use Connectors

There are several connectors on the interior of the board for factory setup and diagnostic use. These are not for customer use.

BOARD LAYOUT

This diagram of the UMAC-CPCI Turbo CPU board shows the locations of the jumpers and connectors. Detailed information about each of the jumpers and connectors follows.



UMAC-CPCI Turbo CPU Board Layout

JUMPER DESCRIPTIONS

Note:

Pin 1 of an E-point is masked by an X and a bold square in white ink on the composite side, and by a square solder pad on the solder side.

E0: Reset-Lock Enable (Factory Use Only)

E Point & Physical Layout	Location	Description	Default
		Jump pins 1 and 2 to lock the UMAC-CPCI Turbo CPU board in the "reset" state to permit installation of on-board logic. This setting for factory use only. Remove jumper to permit normal operation of board.	No jumper installed

E1A: Servo and Phase Clock Direction Control

E Point & Physical Layout	Location	Description	Default
		Jump pins 1 and 2 or remove jumper for the UMAC-CPCI system to use its internally generated servo and phase clock signals and to output these signals on the field wiring connector on the CPU board. E1B should connect pins 2 and 3 or be removed. Jump pins 2 and 3 for the UMAC-CPCI system to expect to receive its servo and phase clock signals on J2 field-wiring connector on the Turbo CPU board. E1B should also connect pins 1 and 2.	Pins 1-2 jumpered

E1B: Servo/Phase Clock Source Control

E Point & Physical Layout	Location	Description	Default
		Jump pin 1 to 2 to get phase and servo clocks from J7 RS422 connector (from an external source such as another UMAC). Jump pin 2 to 3 to get phase and servo clocks from J1 backplane connector (from an ACC-24C2x, or equivalent board). Remove jumper to get phase and servo clocks from J2 Stack connector (from an ACC-2E or equivalent board)	Pins 2 – 3 jumpered

E2: (Reserved for Future Use)

E Point & Physical Layout	Location	Description	Default
			No jumper installed

E3: Re-Initialization on Reset Control

E Point & Physical Layout	Location	Description	Default
		Remove jumper for normal reset mode (default). Jump pins 1 to 2 for re-initialization on reset.	No jumper installed

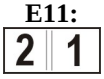
E4: (Reserved for Future Use)

E Point & Physical Layout	Location	Description	Default
			No jumper installed

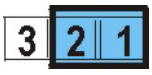
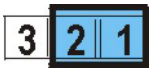
E5: USB/Ethernet Communication Jumper

E Point & Physical Layout	Location	Description	Default
		Jump 1-2 for Ethernet or USB communications from J7 (Ethernet connector) or J3 (USB connector). Jump 2-3 for Ethernet or USB communications through the back J2 connector	Factory installed

E11: Power Supply Check Control

E Point & Physical Layout	Location	Description	Default
E11: 		Jump E11 pin 1 to 2 to include the +12V and –12V analog supplies from the J1 backplane connector in the power-supply check circuit, inhibiting outputs if these supplies fail. Remove E11 jumper so only 5V digital supply is used in power-supply check circuit.	No jumper installed

E17 – E18: Serial Port Select

E Point & Physical Layout	Location	Description	Default
E17: 		Jump E17 pin 1 to 2 to select RS-232 serial data input for main serial port (J4 front-panel or J2 backside connector). Jump E17 pin 2 to 3 to select RS-422 serial data input for main serial port (J4 front-panel or J2 backside connector).	Pins 1-2 jumpered
E18: 		Jump E18 pin 1 to 2 to select RS-232 serial handshake input for main serial port (J2 backside connector only). Jump E18 pin 2 to 3 to select RS-422 serial handshake input f for main serial port (J2 backside connector only).	Pins 1-2 jumpered

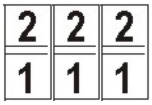
E18A, B, C, D: Ethernet Communication Control

E Point & Physical Layout	Location	Description	Default
1 ☐ ○ ○ E18D 1 ☐ ○ ○ E18C 1 ☐ ○ ○ E18B		Jump 1 to 2 to Ethernet Connection to J7 front connector Jump 2-3 for Ethernet connection through back J2 connector	Pins 1-2 jumpered

E19: Watchdog Disable Jumper

E Point & Physical Layout	Location	Description	Default
		Jump pin 1 to 2 to disable Watchdog timer (for test purposes only.). Remove jumper to enable Watchdog timer.	No jumper installed

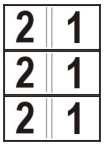
E20 – E22: Power-Up/Reset Load Source

E Point & Physical Layout	Location	Description	Default
E20: 		To load active memory from flash IC on power-up/reset, Remove jumper E20; Jump E21 pin 1 to 2; Jump E22 pin 1 to 2. Other combinations are for factory use only; the board will not operate in any other configuration.	No E20 jumper installed E21 and E22 jump pin 1 to 2

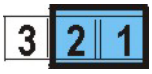
E23: Firmware Reload Enable

E Point & Physical Layout	Location	Description	Default
		Jump pin 1 to 2 to reload firmware through serial or host bus port. Remove jumper for normal operations.	No jumper installed

E25A, B, C: Flash Memory Firmware Bank Select

E Point & Physical Layout	Location	Description	Default
		Remove all jumpers to select standard factory-installed bank of operational firmware. Install one or more jumper(s) to select alternate bank of operation firmware to install (E23 ON) or use (E23 OFF).	No jumpers installed

W1: Flash IC Power Supply Select Jumper

E Point & Physical Layout	Location	Description	Default
	**B-1**	(Note: This jumper is set at the factory and possibly hard soldered. Users should not change this jumper.) Jump pin 1 to 2 to select 3.3V supply for flash memory IC in U10. Jump pin 2 to 3 to select 5V supply for flash memory IC in U10.	Setting dependent on flash IC used.

CONNECTOR SUMMARY

J1:	*****	Compact UBUS Backplane Connector
J2:	*****	"Thru-Backplane" Field Wiring Connector
J4:	*****	RS-232 Front-Panel Serial-Port Connector
J5:		JTAG/OnCE (for factory use only): 10-pin IDC connector
J6:		JISP (for factory use only): 8-pin SIP connector
J10:		JISP_B (for factory use only) 8-pin SIP connector
J11:		First component-side stack connector to CPCI bridge board
J11A:		First solder-side stack connector to CPCI bridge board
J12:		First component-side stack connector to CPCI bridge board
J12A:		First solder-side stack connector to CPCI bridge board

***** Pinouts shown in next section. Connectors not flagged with an asterisk are for internal use or factory setup.

CONNECTOR PINOUTS

Compact UBUS Connector (J1) Pin-Out

Row	Z	A	B	C	D	E	F
25	GND	5V			3.3V	5V	GND
24	GND	BD02	5V	V(I/O)	BD01	BD00	GND
23	GND	3.3V	BD05	BD04	5V	BD03	GND
22	GND	BD09	BD08	3.3V	BD07	BD06	GND
21	GND	3.3V	BD13	BD12	BD11	BD10	GND
20	GND	BD17	GND	BD16	BD15	BD14	GND
19	GND	3.3V	BD20	BD19	GND	BD18	GND
18	GND	BD23	GND	3.3V	BD22	BD21	GND
17	GND	3.3V	{BD26}	{BD25}	GND	{BD24}	GND
16	GND	{BD30}	GND	{BD29}	{BD28}	{BD27}	GND
15	GND	3.3V	BWR-	BRD-	GND	{BD31}	GND
14	(KEY)	(KEY)	(KEY)	(KEY)	(KEY)	(KEY)	(KEY)
13	(KEY)	(KEY)	(KEY)	(KEY)	(KEY)	(KEY)	(KEY)
12	(KEY)	(KEY)	(KEY)	(KEY)	(KEY)	(KEY)	(KEY)
11	GND	CS10-	CS4-	CS3-	GND	CS2-	GND
10	GND	CS16-	GND	3.3V	CS14-	CS12-	GND
9	GND	IREQ2-	IREQ1-	MEMCS1-	GND	MEMCS0-	GND
8	GND	PHASE+	GND	SERVO+	WAIT-	IREQ3-	GND
7	GND	PHASE-	WDO	SERVO-	GND		GND
6	GND	BA02	GND	3.3V	BA01	BA00	GND
5	GND	BA04	BA03	RESET-	GND	BX/Y	GND
4	GND	BA07	GND	V(I/O)	BA06	BA05	GND
3	GND	BA11	BA10	BA09	5V	BA08	GND
2	GND	{BA15}	5V	{BA14}	BA13	BA12	GND
1	GND	5V	-12V	PWRGUD	+12V	5V	GND

Notes:

1. Row 25 is physically at the top of the connector in its “normal” orientation; Row 1 is at the bottom. Looking from the front of the rack, Column Z is on the left; Column F is on the right.
2. Supply (Vxx & xxV) and ground pins are in the same locations as the Compact PCI bus.
3. Spaces marked *(KEY)* are for the mechanical key; these are not pins.
4. Pins marked with {} brackets are reserved for future use; the signals inside the brackets are proposed for future expansion to a 32-bit data bus and 16-bit address bus.

UMAC-CPCI Turbo CPU Board J2 Connector

Row	Z	A	B	C	D	E	F
22	GND			+5V			GND
21	GND	RxD/	CTS	+5V	TxD/	RTS	GND
20	GND	RD-	RD+	GND	SD-	SD+	GND
19	GND	CS+	CS-	GND	RS+/	RS-	GND
18	GND	DSR	DTR		INIT/		GND
17	GND	SERVO-	SERVO+		PHASE-	PHASE+	GND
16	GND						GND
15	GND	AuxRxD/	AuxCTS		AuxTxD/	AuxRTS	GND
14	GND	AuxDSR	AuxDTR				GND
13	GND		USBDP (D+)	GND	USBDM (D-)		GND
12	GND						GND
11	GND	EthTxF+	EthTxF-		EthRxF+	EthRxF-	GND
10	GND						GND
9	GND						GND
8	GND						GND
7	GND						GND
6	GND						GND
5	GND						GND
4	GND						GND
3	GND						GND
2	GND		WD_NO	WD_COM	WD_NC		GND
1	GND						GND

Notes:

1. Row 25 is physically at the top of the connector in its "normal" orientation; Row 1 is at the bottom. Looking from the front of the rack, Column Z is on the left; Column F is on the right.
2. The RxD/, CTS, TxD/, and RTS lines are standard RS-232 signals. The inputs are only used if jumpers E17 and E18 each connect their pins 1 and 2. The DSR and DTR lines are simply shorted together.
3. The RD-, RD+, SD-, SD+, CS+, CS-, RS+, and RS- lines are standard RS-422 signals. The inputs are only used if jumpers E17 and E18 each connect their pins 2 and 3.
4. The SERVO-, SERVO+, PHASE- and PHASE+ clock lines are at RS-422 levels. These signals are outputs if jumper E1A connects its pins 1 and 2; they are inputs if jumper E1A connects pins 2 and 3.
5. The AuxRxD/, AuxCTS, AuxTxD/, and AuxRTS lines are standard RS-232 signals. These signals are provided only if the Option 9T auxiliary serial port is ordered. The AuxDSR and AuxDTR lines are simply shorted together.
6. The USBDP(D+) and USBDM(D-) signals are standard USB signals. They are only provided if the Option 1A USB interface is ordered.
7. The EthTxF+, EthTxF-, EthRxF+, and EthRxF- signals are standard Ethernet signals. They are only provided if the Option 1 Ethernet interface is ordered.
8. The WD_NO (normally open), WD_COM (common) and WD_NC (normally closed) lines are the outputs of the watchdog-timer hard-contact relay. The normally open contact is only conducting to common if the card is powered and operating correctly. The normally closed contact is only conducting to common if the card is not powered or the watchdog timer has tripped.

J4: RS-232 Serial Port Connector

(DB-9S Connector)

Pin #	Symbol	Function	Description	Notes
1	N.C.		No connect	
2	TXD-	Output	Send Data	Low TRUE
3	RXD-	Input	Receive Data	Low TRUE
4	DSR	Bidirect	Data Set Ready	Shorted to DTR
5	GND	Common	UMAC CPCI Reference	
6	DTR	Bidirect	Data Terminal Ready	Shorted to DSR
7	CTS	Input	Clear to Send	High TRUE
8	RTS	Output	Request to Send	High TRUE
9	N.C.		No connect	
Jumpers E17 and E18 should connect pins 1 and 2 to use this port for RS-232 communications; they should connect pins 2 and 3 to use this port for RS-422 communications.				

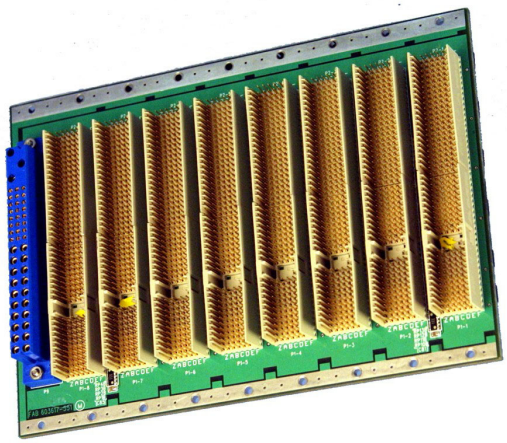
ACCESSORIES

The UMAC-CPCI Turbo CPU board is always used with accessory boards. Delta Tau provides several accessory boards in the UMAC-CPCI family that can be used with the CPU board; other parties may produce accessory boards as well. Each accessory board has its own hardware reference manual.

ACC-Cx Compact UBUS Backplane Boards

The ACC-Cx family of Compact UBUS backplane boards provides the means for the CPU board to communicate with other accessory boards. The x in the name of the backplane board refers to the number of backplane data slots provided.

This picture shows an ACC-C8 8-slot backplane board. It has a P47-style power connector suitable for a standard 1-slot CPCI-format power supply.

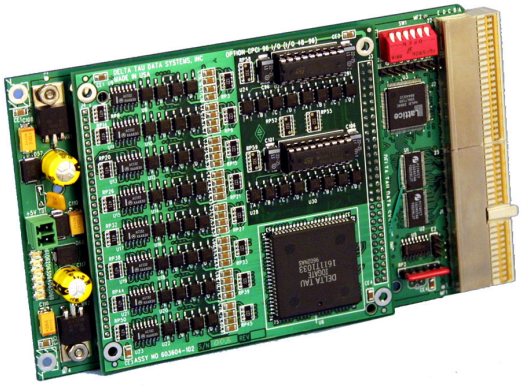


ACC-8CR Test Breakout Board

The ACC-8CR board provides a behind-the-backplane breakout scheme for the J2 field wiring connector on any of the 3U-format UMAC-CPCI board. It is designed to plug into the rear of an ACC-Cx Compact UBUS backplane board, and it meets the Compact PCI physical specification (100mm x 80mm) for rear distribution boards. It has 110 screw-down terminal points, one for each signal on the J2 field wiring connector.

ACC-11C Sinking I/O Board

The ACC-11C board provides 32 isolated 12V-24V sinking inputs and 16 isolated sinking outputs up to 24V and 100mA per output. With its Option 1 mezzanine board, an additional 32 inputs and 16 outputs are provided, for a total of 96 I/O points in a single slot.

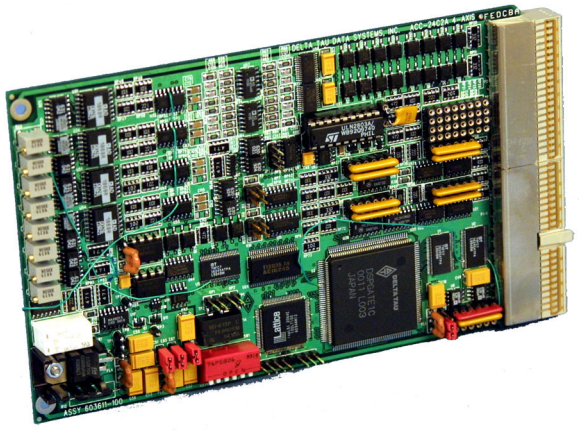


ACC-24C2 PWM Axis Board

The ACC-24C2 PWM axis board provides the interface circuitry for 4 axes of purely digital control in a single slot, with direct PWM outputs, serial ADC inputs, quadrature encoder inputs, and input/output flags. Because of pin limitations on the J2 field wiring connector, signals that are differential on other ACC-24x2 boards are single-ended here. To take these signals any significant distance, differential line drivers and receivers are required on a distribution board.

ACC-24C2A Analog Axis Board

The ACC-24C2A analog axis board provides the interface circuitry for 4 axes of control in a single slot, with analog interface to the servo drives. It also has one pulse-and-direction output per axis for stepper drives, or stepper-replacement servo drives. One 18-bit D/A converter comes standard for each axis; Option 1 provides a second D/A converter per axis, which can be used as part of a "sine-wave" control scheme, or for non-servo use. Option 2 provides eight 12-bit A/D converters.



ACC-51C Analog Encoder Interpolator Board

The ACC-51C provides the circuitry for the high-resolution interpolation of 2 or 4 analog sine/cosine encoders, yielding 4096 states per line of the encoder. The board comes standard with two channels of interface; Option 1 provides two additional channels.

SCHEMATICS

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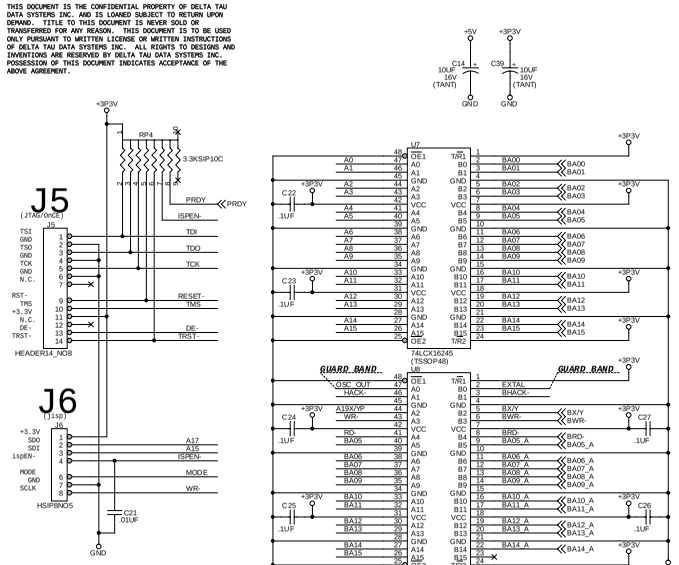
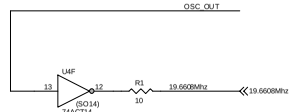
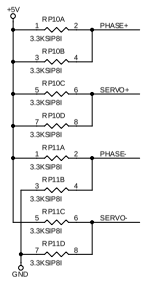
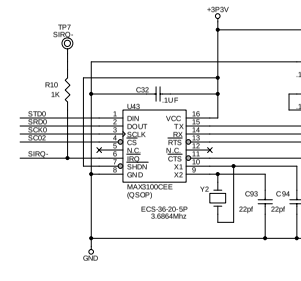
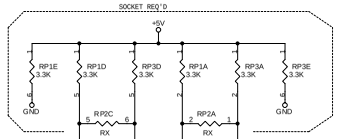
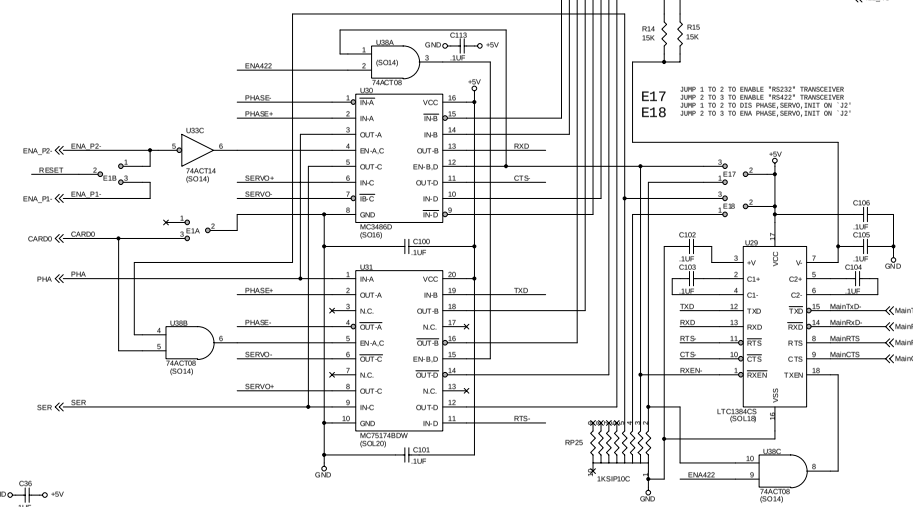


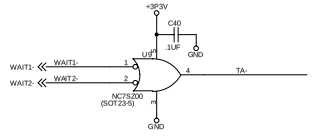


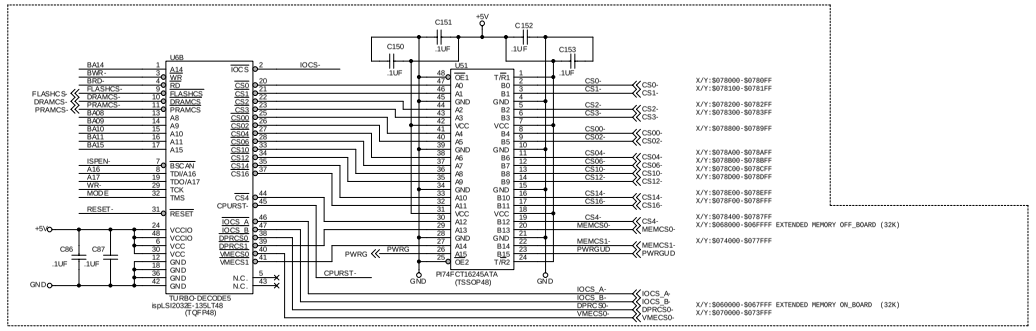


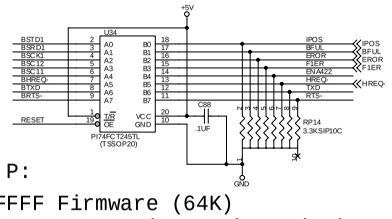


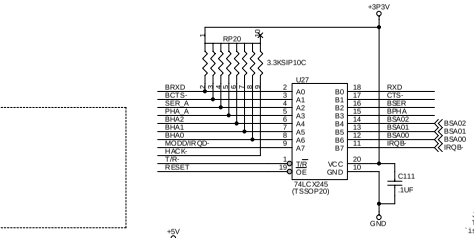


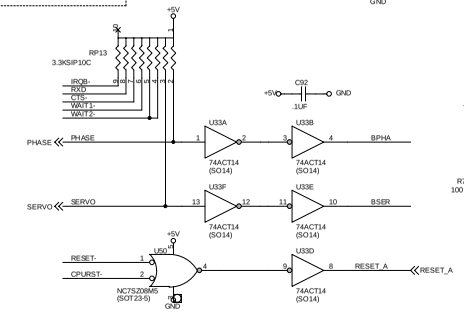


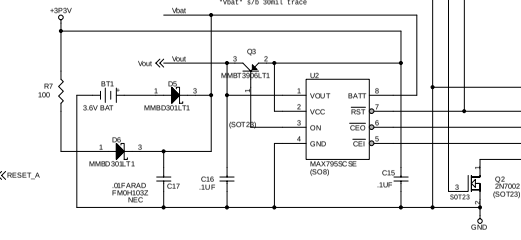


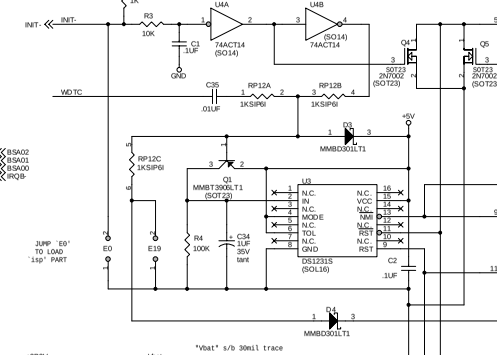


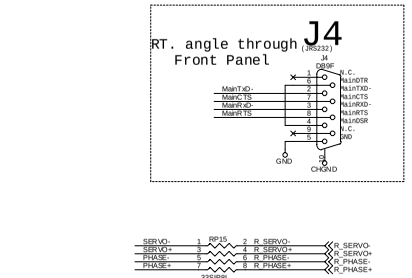












PRAM MEMORY P:

```
$000000-$00FFFF Firmware (64K)
$040000-$0403FF User Written Phase (1K)
$040400-$040BFF User Written Servo (2K)
$050000-$05FFFF Plcc Standard Memory Option (64K)
$050000-$0BFFFF Plcc Extended Memory Option (448K)
```

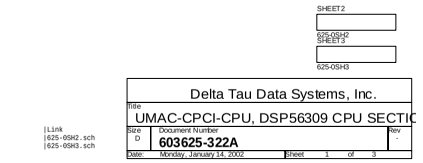
NOTE:

```
E1A 2 TO 1 = ENABLE  'CARD0'
E1A 2 TO 3 = DISABLE 'CARD0'

E1B 2 TO 1  ON = ENABLE  'PHASE & SERVO' FROM 'P2'
E1B 2 TO 1  OFF = DISABLE  PHASE & SERVO' FROM 'P2'

E1B 2 TO 3  ON = ENABLE  'PHASE & SERVO' FROM 'P1'
E1B 2 TO 3  OFF = DISABLE  PHASE & SERVO' FROM 'P1'

E1B EMPTY = ENABLE  'PHASE & SERVO' FROM 'J12/J12A'
```



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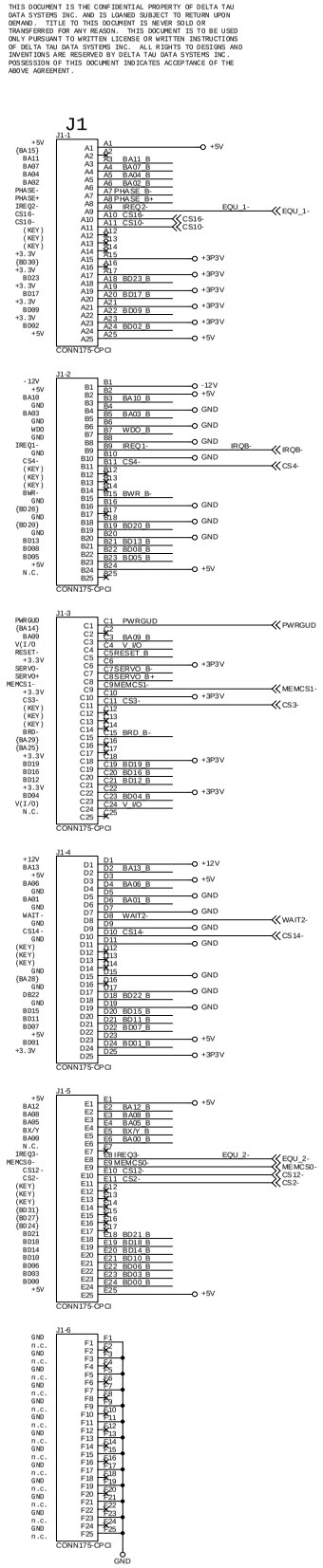

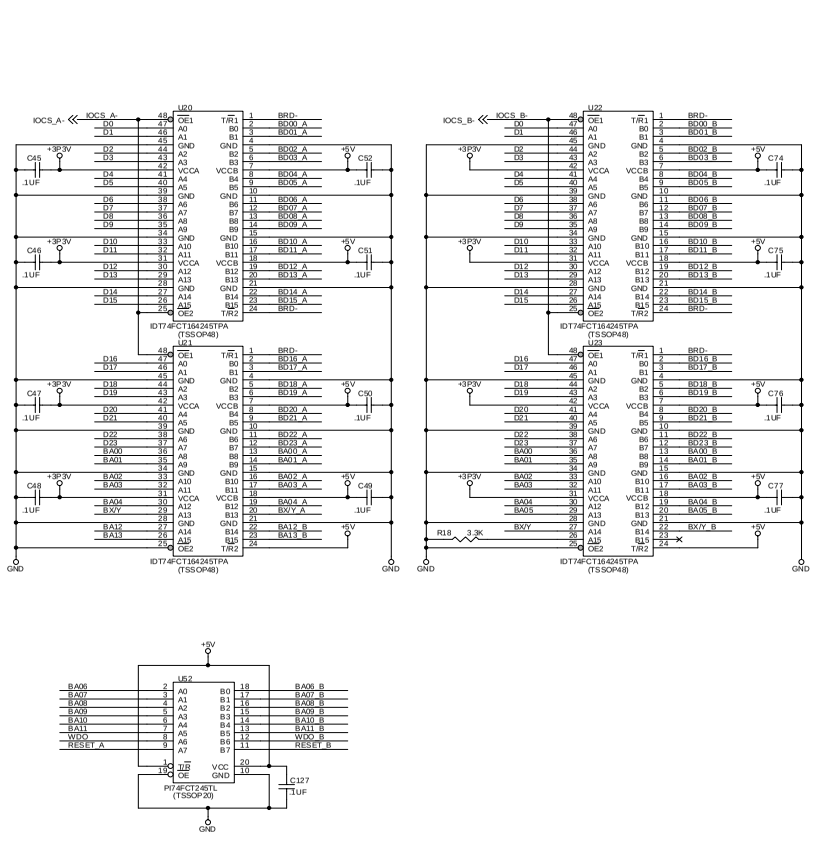

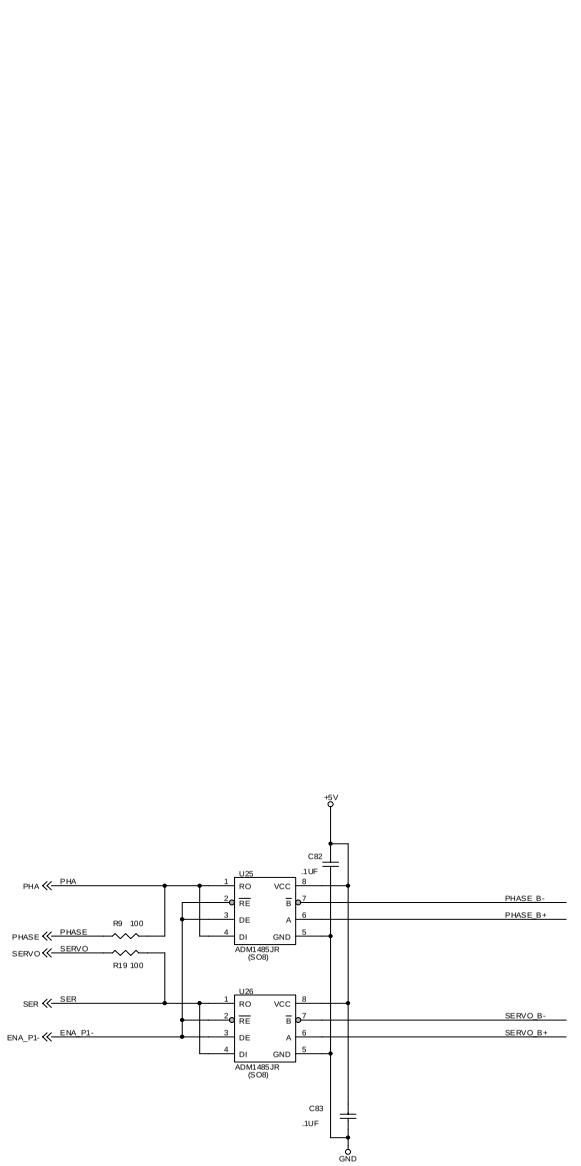

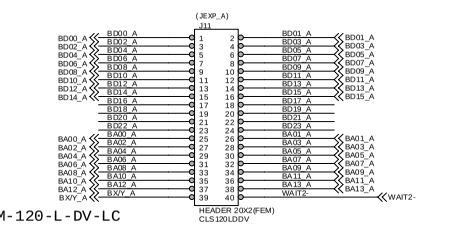

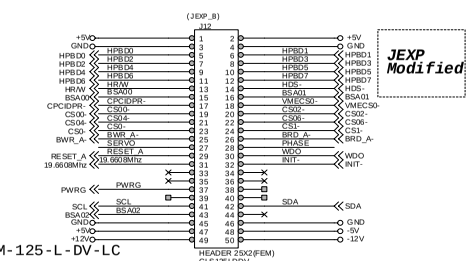

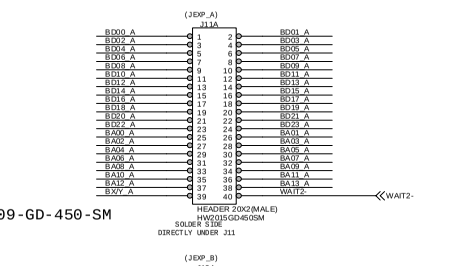

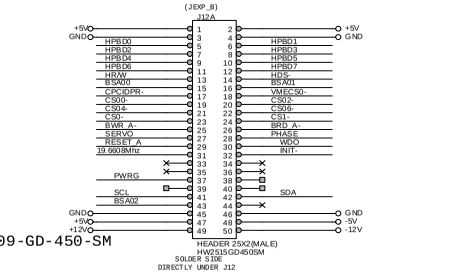

Delta Tau Data Systems, Inc.		
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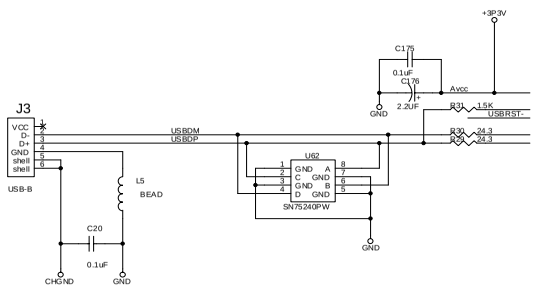
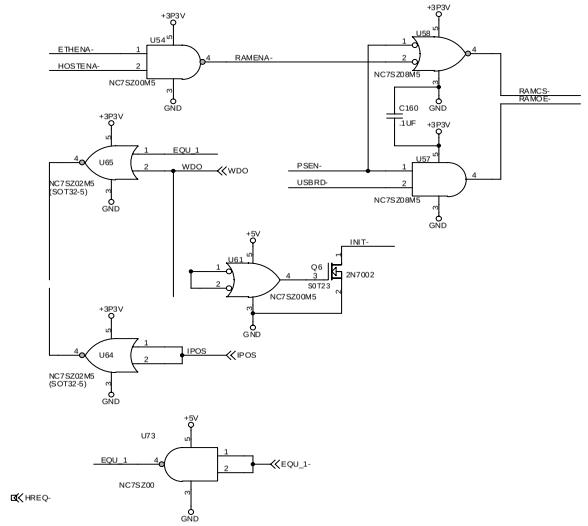
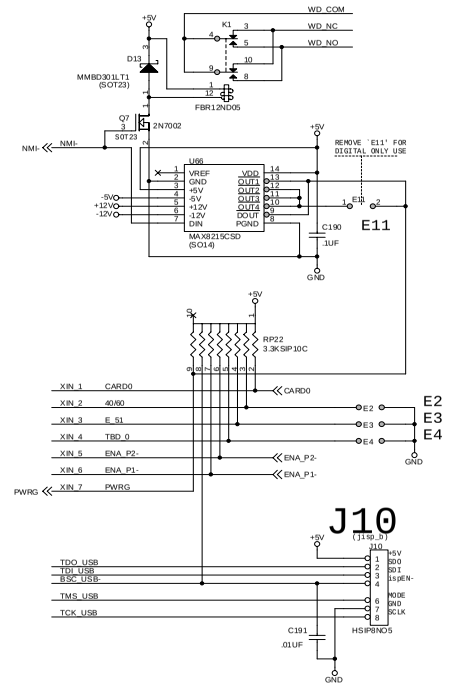
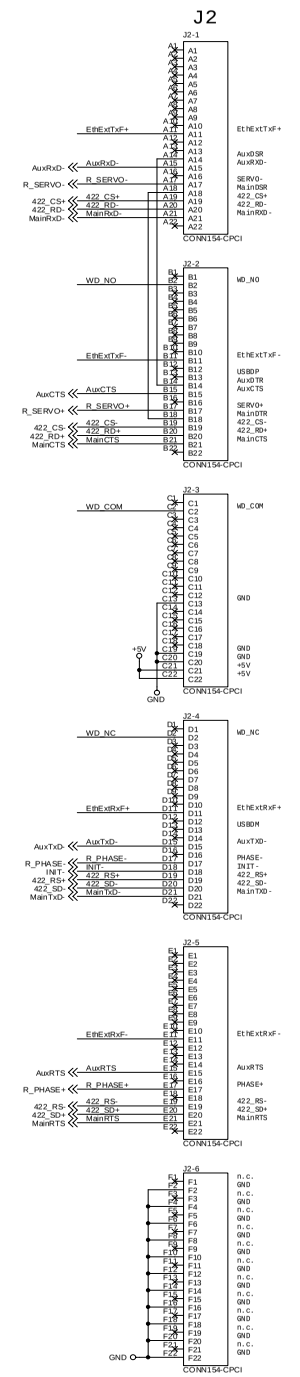
Size: D	Document Number: 603625-322A	Rev: -
Date: Tuesday, January 15, 2002	Sheet 2 of 3	

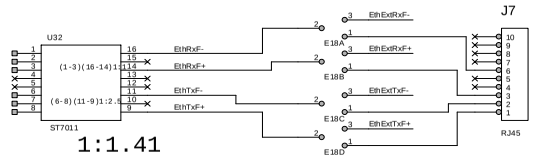


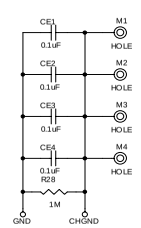


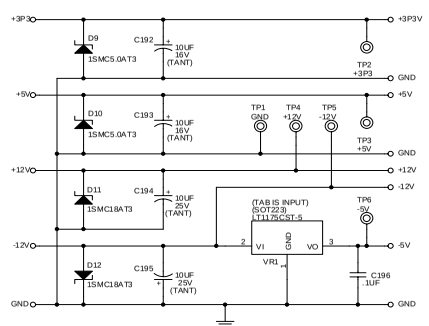




OPTION 1
Ethernet Option







Delta Tau Data Systems, Inc.
2.0/Ethernet UMAC-CPCI Communication

Title: UMAC-CPCI-CPU, USB/2.0/Ethernet Secti

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Date: Tuesday, January 15, 2002 | Sheet 3 of 3